A Comprehensive Thermal Solution in Advanced Large Scale 3DIC Design

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INTRODUCTION

Narrower physical wires, higher current density, increasing impact of wire temperature on EM limit, all these factors can lead to rise of the chip temperature and worsen the electromigration(EM) phenomenon, such as open or short. To avoid function failure caused by reliability-related problems, designer restricts the design excessively with whole die set to a value higher than the maximum operating temperature in traditional flow, which causes difficulty to iterate and even failure to sign-off. So the accurate "Thermal aware EM sign-off" is a must for advanced 3DIC design.

Different from the traditional flow, our flow can model the realistic heat dissipation environment of the complicated 3DIC accurately, and meanwhile take the thermal coupling of the instance, and the wire-to-wire joule heat into account to analyze the thermal convergence process precisely. With the thermal-aware EM flow, we can avoid over-design and under-design. And the simulation results can be used to provide guidance for the heat dissipation design of the system.

DESIGN

Table 1. Input Data

	Item	Size	RedHawk-SC Electrothermal（ET）
Backend	die_0	~25 mm*14 mm	Detail CTM
	die_1	~25 mm*14 mm	Detail CTM
	InFO	~26mm*31mm	Detail CTM
	C4 bump	~0.4M	
Pkg/System	PKG	icepeak-Model	Boundary condition
	PCB	icepeak-Model	Boundary condition
	Heat Sink	icepeak-Model	Boundary condition

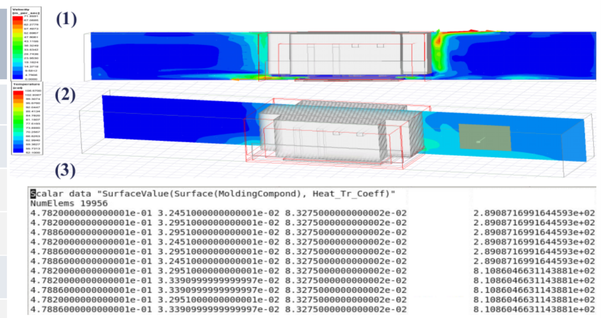


Figure 1. RHSC-ET Thermal Results with Icepak Boundary Condition

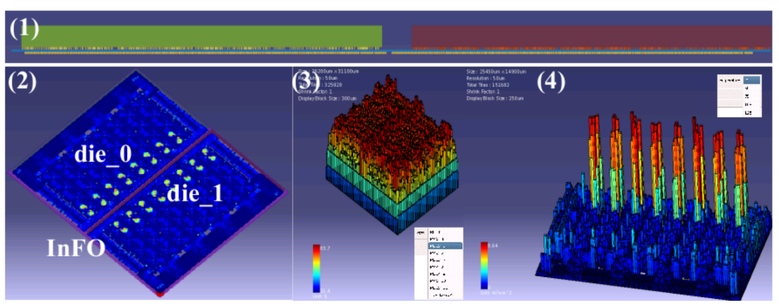
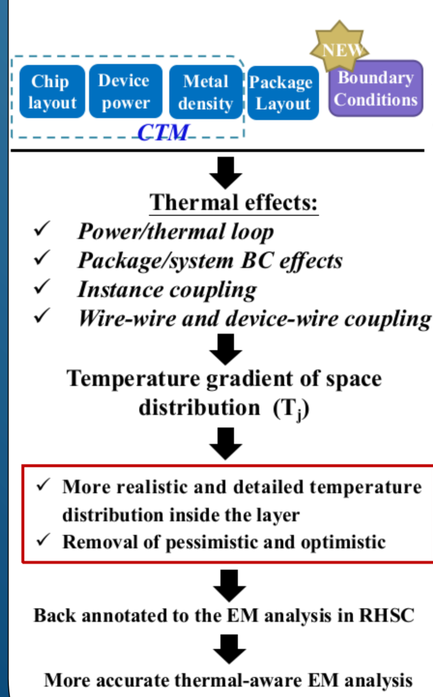


Figure 2.
1). and 2). Structure diagram of 3DIC stack-up components
3). Tile-based metal density distribution in InFO CTM
4). Tile-based temperature-dependent power distribution in logic die CTM



A. Design:

Dies: The design stack-up is consisted of two dies.

System: These dies are interconnected via InFO (Integrated Fan-Out, InFO). Package, PCB and other system components are taken into consideration.

B: Simulation flow:

- Generate a tile-based power distribution model at the micron level of each die and InFO.
- Perform the joint heat dissipation simulation of the system, and then generate a heat exchange file as boundary condution
- Based on the above input files, Redhawk_SC_ET do thermal analysis and generates detailed temperature distribution gradient files for different layers and locations.
- Replace the unified temperature setting with detailed temperature profile, and perform EM simulation.

RESULT & BENEFITS

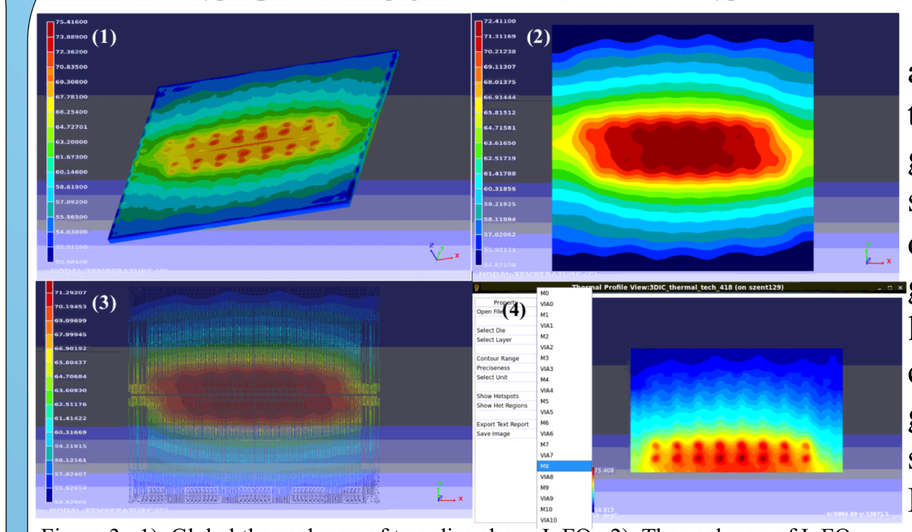


Figure 3. 1). Global thermal map of two dies above InFO 2). Thermal map of InFO 3). Thermal map of C4 bump 4). Per layer chip Thermal profile

For different layers and locations, different temperatures (Tj) are generated. The realistic spatial tempatrue distribution scenario generated by system-level thermal analysis can replace the coarse global temperature setting in traditional EM analysis flow.

When the actual temperature is higher than the coarse global temperature， the violations need to be fixed to a greater extent to avoid product failure or enhance heat dissipation design. In our case, the real ambient temperature on die_0 and die_1 chip are below 75°C due to the very good thermal conditions on the system. So the EM percentage in the same wire get a significant decrease with the thermal profile. This helps us iterate EM faster and reduce pessimism.

Traditional EM result VS. Thermal Aware EM result >> EM violation decrease << temperature decrease

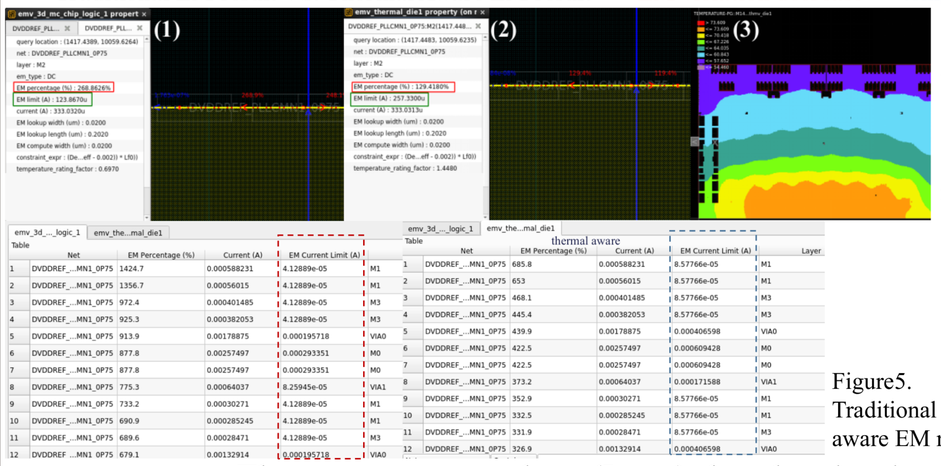


Figure 4.
1) and 2) EM attribute of the same wire
1).Traditional EM result 268.86%
2).Thermal aware EM result 129.41%
3). Temperature distribution of one layer in Redhawk_SC

Figure5.
Traditional EM result VS. Thermal aware EM result of same wire

Table 2. EM limit derate-Factor VS temperature

Temp (°C)	Derate
100	1.073
105	1
110	0.927
115	0.855
120	0.782
125	0.71
130	0.637
135	0.565
140	0.492
145	0.419
150	0.347

Referenced from other documents

The max current values (Imax) that the circuit can tolerate which means EM limit degrade with increasing temperature. The higher the temperature, the more severe the degradation, as shown in Table 2. When the actual system temperature is lower than the general simulation temperature, the wires can bear larger current. In this way, we can obtain better results.

1. Reduce the number of false EM violations due to the pessimistic assumptions of global temperature.
2. Increase the design frequency to obtain higher performance.
3. Reduce the wire width to release winding resources for more critical parts, to obtain better performance-power-area (PPA).
4. Reduce the cost in heat dissipation to reduce product costs and iteration period.

SUMMARY

- For 2.5D/3DIC design, chip-centric thermal analysis with accuracy system boundary condition from Icepak is very important to obtain realistic thermal profile.
- Using spatial distribution temperature information which represent the realistic ambient temperature to avoid over-design and under-design.
- It is important to assess EM margins and optimal thermal dissipation of the whole stacked multi-die, package and board across a wide range of operating conditions and modes.